AFZAL MALIK

Bachelor of Technology
Electronics Engineering
Aligarh Muslim University (NIRF Rank: 8), Aligarh, U.P

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GitHub
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Education

Degree	Institute	Board / University	Percentage	Year
B.Tech (ECE)	Zakir Husain College of Engineering and Technology, Aligarh	Aligarh Muslim University	93.38	2021-2025

Skills

- **Technical Skills**: LT Spice, Circuit Design & simulation, Cadence Virtuoso, Analog Circuit Design, Verilog HDL, Xilinx Vivado, FPGA, Digital System Design, C/C++, Microsoft Office Suite
- **Courses**: VLSI Design & Technology, Analog & Digital Electronics, Digital IC Design, Digital System Design, Control System, Circuit Theory

Internship

- **Analog Circuit Design Intern** *June - July 2023*
  Under mentorship of Dr. GS Javed (Analog Design Manager @Intel) Bangalore, India
  – Designed basic analog circuit building blocks such as current mirrors and operational amplifiers using the gm/Id methodology, and gained experience with EDA tools. — **GitHub**.
  – Tools Used: LT Spice, Electric VLSI, Analog Designer Toolbox (ADT)

Projects

- **Design of Phase-Locked Loop (PLL) | Major Project** *Aug 2024 - Ongoing*
  B.Tech
  – This project involves designing a Phase-Locked Loop (PLL) for a 2.4 GHz frequency in CMOS 180nm Technology.
  – Designing PLL Blocks: Voltage Controlled Oscillator, Phase Frequency Detector, Divider, Charge Pump & Loop Filter
- **Design and FPGA Implementation of Neural Network based Digit Recognition System** *Jan - May 2024*
  B.Tech
  – Tools Used: Xilinx Vivado, VS code | FPGA Board: NEXYS A7 | Language: Verilog HDL & Python
  – Design of software model of Neural Network for Handwritten Digit Recognition system using Python. Hardware realisation of the neural network using Verilog HDL, validating behavioural, Post synthesis & Post Implementation Simulations and then ANN is implemented on FPGA.
- **Design, Simulation and layout of Two-Stage Operational Amplifier** *June - July 2023*
  Analog Circuit Design Intern **GitHub**
  – Tools Used: LT Spice and Analog Designer Toolbox (ADT), Electric Binary.
  – Utilized Gm/Id methodology to design and simulate a Two-Stage Operational Amplifier in the 180 nm technology for the specifications: Gain >1000, Gain Bandwidth Product (GBW) > 1GHz, and Phase Margin of 50.
- **CMOS Inverter Design: From Schematic to GDSII** *Nov 2022 - Sept 2024*
  Self **GPDK90 GitHub** | **TSMC 180nm GitHub**
  – Tools Used: Cadence Virtuoso, LT Spice, Electric Binary
  – Completed schematic design, simulation, analysis, and layout using LT Spice and Electric Binary for TSMC 180nm. Later, using Cadence Virtuoso for GPDK90 technology, Completed schematic design, simulation, analysis, and layout including pre- and post-layout simulations, parasitics extraction, and GDSII generation.

Conference Publications

- **A 5GHz Gain-Bandwidth Op-Amp in 180nm technology** *May 2024*
  4th IEEE International Conference on VLSI Systems, Architecture, Technology, and Applications (VLSI SATA 2024) **IEEE Xplore**

Positions of Responsibility

- **President**,Engineering Design & Implementation Club, ZHCET, AMU *Dec. 2022 - till date*
  – Led the club's activities, organized workshops and hackathons, mentored juniors, and connected with industry professionals

Honors & Awards

–Consistently ranked within the Top 3 students of my batch with an overall CPI of 9.32 *2024*
–Awarded scholarship twice from Lead, Ignite & Transform Scholarship (LIT) program based on Merit. *2022, 23*
–Received University Merit Financial award, Ranked 2nd out of 70 students of Electronics Engineering in 3rd year. *2024*
–Selected as an Analog Circuit Design Intern for Summer Training program in Bangalore organised by EDIC, AMU. *2023*
–Rank 1 in school in Intermediate with 92.8% *2019*